Order this document by MC44602/D

MOTOROLA

MC44602

Advance Information

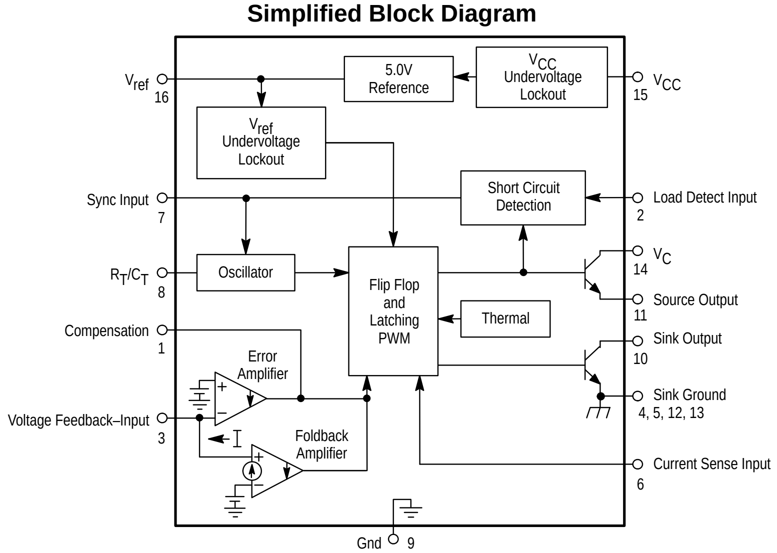
High Performance Current Mode Controller

The MC44602 is an enhanced high performance fixed frequency current mode controller that is specifically designed for off–line and high voltage dc–to–dc converter applications. This device has the unique ability of changing operating modes if the converter output is overloaded or shorted, offering the designer additional protection for increased system reliability. The MC44602 has several distinguishing features when compared to conventional current mode controllers. These features consist of a foldback amplifier for overload detection, valid load and demag comparators with a fault latch for short circuit detection, thermal shutdown, and separate high current source and sink outputs that are ideally suited for driving a high voltage bipolar power transistor, such as the MJE18002, MJE18004, or MJE18006.

Standard features include an oscillator with a sync input, a temperature compensated reference, high gain error amplifier, and a current sensing comparator. Protective features consist of input and reference undervoltage lockouts each with hysteresis, cycle–by–cycle current limiting, a latch for single pulse metering, and a flip–flop which blanks the output off every other oscillator cycle, allowing output deadtimes to be programmed from 50% to 70%. This device is manufactured in a 16 pin dual–in–line heat tab package for improved thermal conduction.

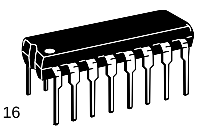
- Separate High Current Source and Sink Outputs Ideally Suited for Driving Bipolar Power Transistors: 1.0 A Source, 1.5 A Sink
- Unique Overload and Short Circuit Protection
- Thermal Protection
- Oscillator with Sync Input
- Current Mode Operation to 500 kHz Output Switching Frequency
- Output Deadtime Adjustable from 50% to 70%
- Automatic Feed Forward Compensation
- Latching PWM for Cycle–By–Cycle Current Limiting
- Input and Reference Undervoltage Lockouts with Hysteresis
- Low Startup and Operating Current

Simplified Block Diagram



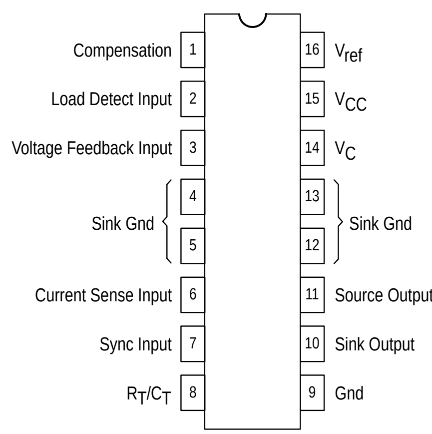
HIGH PERFORMANCE CURRENT MODE CONTROLLER

SEMICONDUCTOR TECHNICAL DATA



P2 SUFFIX
PLASTIC PACKAGE
CASE 648C
DIP (12 + 2 + 2)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44602	T_A = –25 to 85°C	DIP (12 + 2 + 2)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Sink Ground Voltage with Respect to Gnd (Pin 9)	$V_{Sink(neg)}$	–5.0	V
Output Supply Voltage with Respect to Sink Gnd (Pins 4, 5, 12, 13)	V_C	20	V
Output Current (Note 1) Source Sink	 $I_{O(Source)}$ $I_{O(Sink)}$	 1.0 1.5	A
Output Energy (Capacitive Load per Cycle)	W	5.0	µJ
Current Sense and Voltage Feedback Inputs	V_{in}	–0.3 to 5.5	V
Sync Input High State Voltage Low State Reverse Current	 V_{IH} I_{IL}	 5.5 –20	 V mA
Load Detect Input Current	I_{in}	–20 to +10	mA
Error Amplifier Output Sink Current	$I_{EA\ (Sink)}$	10	mA
Power Dissipation and Thermal Characteristics Maximum Power Dissipation at T_A = 25°C Thermal Resistance, Junction–to–Air Thermal Resistance, Junction–to–Case	 P_D $R_{\theta JA}$ $R_{\theta JC}$	 2.5 80 15	 W °C/W °C/W
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature	T_A	–25 to +85	°C

NOTE: 1. Maximum package power dissipation limits must be observed.

ELECTRICAL CHARACTERISTICS (V_{CC} and V_C = 12 V [Note 2], R_T = 10k, C_T = 1.0 nF, for typical values T_A = 25°C, for min/max values T_A = –25°C to +85°C [Note 3] unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER SECTION					
Voltage Feedback Input (V_O = 2.5V)	V_{FB}	2.45	2.5	2.65	V
Input Bias Current (V_{FB} = 2.5 V)	I_{IB}	–	–0.6	–2.0	µA
Open Loop Voltage Gain (V_O = 2.0 V to 4.0 V)	A_{VOL}	65	90	–	dB
Unity Gain Bandwidth T_J = 25°C T_A = –25 to +85°C	BW	 1.0 0.8	 1.4 –	 1.8 2.0	MHz
Power Supply Rejection Ratio (V_{CC} = 10 V to 16 V)	PSRR	65	70	–	dB
Output Current Sink (V_O = 1.5 V, V_{FB} = 2.7 V) T_J = 25°C T_A = –25 to +85°C Source (V_O = 5.0 V, V_{FB} = 2.3 V) T_J = 25°C T_A = –25 to +85°C	 I_{Sink} I_{Source}	 – 1.5 – –2.0	 5.0 – –1.1 –	 – 10 – –0.2	mA
Output Voltage Swing High State ($I_{O(Source)}$ = 0.5 mA, V_{FB} = 2.3 V) Low State ($I_{O(Sink)}$ = 0.33 mA, V_{FB} = 2.7 V)	 V_{OH} V_{OL}	 6.0 –	 7.0 1.0	 – 1.1	V

NOTES: 2. Adjust V_{CC} above the startup threshold before setting to 12V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

ELECTRICAL CHARACTERISTICS (V_{CC} and V_C = 12 V [Note 2], R_T = 10k, C_T = 1.0 nF, for typical values T_A = 25°C, for min/max values T_A = –25°C to +85°C [Note 3] unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR SECTION					
Frequency T_J = 25°C T_A = –25°C to +85°C	f_{OSC}	 168 160	 180 –	 192 200	kHz
Frequency Change with Voltage (V_{CC} = 12 V to 18 V)	$\Delta f_{OSC}/\Delta V$	–	0.1	0.2	%/V
Frequency Change with Temperature	$\Delta f_{OSC}/\Delta T$	–	0.05	–	%/°C
Oscillator Voltage Swing (Peak–to–Peak)	$V_{OSC(pp)}$	1.3	1.6	–	V
Discharge Current (V_{OSC} = 3.0 V) T_J = 25°C T_A = –25°C to +85°C	I_{dischg}	 6.5 6.0	 10 –	 13.5 14	mA
Sync Input Threshold Voltage High State Low State	 V_{IH} V_{IL}	 2.5 1.0	 2.8 1.3	 3.2 1.7	V
Sync Input Resistance T_J = 25°C T_A = –25°C to +85°C	R_{in}	 6.5 6.0	 10 –	 13.5 18	kΩ
REFERENCE SECTION					
Reference Output Voltage (I_O = 1.0 mA)	V_{ref}	4.7	5.0	5.3	V
Line Regulation (V_{CC} = 12 V to 18 V)	Reg_{line}	–	1.0	10	mV
Load Regulation (I_O = 1.0 mA to 20 mA)	Reg_{load}	–	3.0	15	mV
Temperature Stability	T_S	–	0.2	–	mV/°C
Total Output Variation over Line, Load and Temperature	V_{ref}	4.65	–	5.35	V
Output Noise Voltage (f = 10 Hz to 10 kHz, T_J = 25°C)	V_n	–	50	–	μV
Long Term Stability (T_A = 125°C for 1000 Hours)	S	–	5.0	–	mV
Output Short Circuit Current T_J = 25°C T_A = –25°C to +85°C	I_{SC}	 – –70	 –130 –	 – –180	mA
CURRENT SENSE SECTION					
Current Sense Input Voltage Gain (Notes 4 & 5) T_J = 25°C T_A = –25°C to +85°C	A_V	 2.85 2.7	 3.0 –	 3.15 3.2	V/V
Maximum Current Sense Input Threshold (Note 4)	V_{th}	0.9	1.0	1.1	V
Input Bias Current	I_{IB}	–	–4.0	–10	μA
Propagation Delay (Current Sense Input to Sink Output)	$t_{PLH(in/out)}$	–	100	150	ns
UNDERVOLTAGE LOCKOUT SECTIONS					
Startup Threshold (V_{CC} Increasing)	V_{th}	13	14.1	15	V
Minimum Operating Voltage After Turn–On (V_{CC} Decreasing)	$V_{CC(min)}$	9.0	10.2	11	V
Reference Undervoltage Threshold (V_{ref} Decreasing)	$V_{ref}(UVLO)$	3.0	3.35	3.7	V

NOTES: 2. Adjust V_{CC} above the startup threshold before setting to 12V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
4. This parameter is measured at the latch trip point with I_{FB} = –5.0 μA, refer to Figure 9.
5. Comparator gain is defined as $A_V = \frac{\Delta V\ \text{Compensation}}{\Delta V\ \text{Current Sense Input}}$

ELECTRICAL CHARACTERISTICS (V_{CC} and V_C = 12 V [Note 2], R_T = 10k, C_T = 1.0 nF, for typical values T_A = 25°C, for min/max values T_A = –25°C to +85°C [Note 3] unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUT SECTION					
Output Voltage (T_A = 25°C)					V
Low State (I_{Sink} = 100 mA)	V_{OL}	–	0.6	0.3	
(I_{Sink} = 1.0A)		–	1.8	2.0	
(I_{Sink} = 1.5 A)		–	2.1	2.6	
High State (I_{Source} = 50 mA)	(V_{CC}–V_{OH})	–	1.4	1.7	
(I_{Source} = 0.5 A)		–	1.7	2.0	
(I_{Source} = 0.75 A)		–	1.8	2.2	
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{Sink} = 1.0 mA)	$V_{OL(UVLO)}$	–	0.1	1.1	V
Output Voltage Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	–	50	150	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	–	50	150	ns
PWM SECTION					
Duty Cycle					%
Maximum	$DC_{(max)}$	46	48	50	
Minimum	$DC_{(min)}$	–	–	0	
TOTAL DEVICE					
Power Supply Current	I_{CC}				mA
Startup (V_{CC} = 5 V)		–	0.2	0.5	
Operating (Note 2)					
T_J = 25° C		–	17	20	
T_A = –25°C to +85° C		10	–	22	
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	18	20	23	V
OVERLOAD AND SHORT CIRCUIT PROTECTION					
Foldback Amplifier Threshold (Figures 9,10)	ΔV_{FB}	(V_{FB}–100)	(V_{FB}–200)	(V_{FB}–300)	mV
Load Detect Input					
Valid Load Comparator Threshold ($V_{Pin\ 2}$ Increasing)	$V_{th(VL)}$	2.0	2.5	3.0	V
Demag Comparator Threshold ($V_{Pin\ 2}$ Decreasing)	$V_{th(Demag)}$	50	88	120	mV
Propagation Delay (Input to Sink or Source Output)	$t_{PLH(in/out)}$	–	1.1	1.6	µS
Input Resistance	R_{in}	12	18	30	kΩ

NOTES: 2. Adjust V_{CC} above the startup threshold before setting to 12V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

Figure 1. Timing Resistor versus Oscillator Frequency

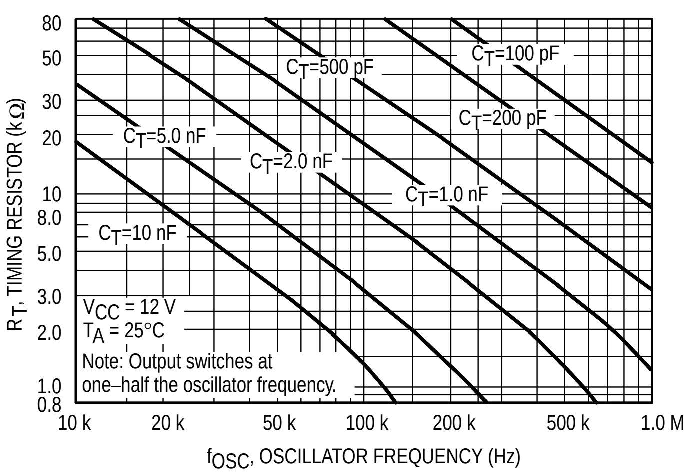


Figure 2. Output Deadtime versus Oscillator Frequency

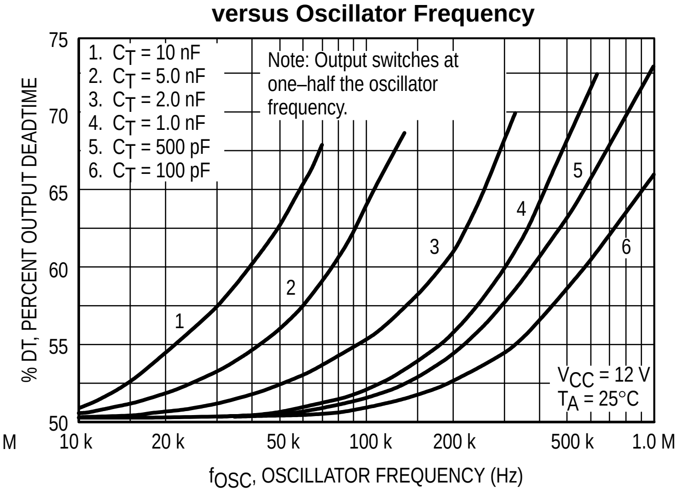


Figure 3. Oscillator Discharge Current versus Temperature

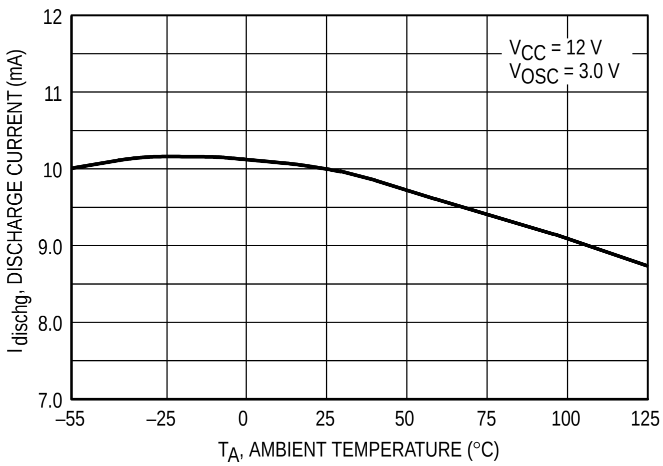


Figure 4. Oscillator Voltage Swing versus Temperature

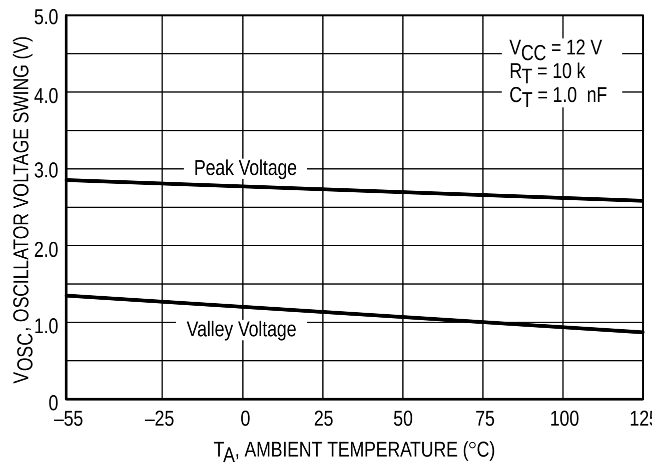


Figure 5. Error Amp Small Signal Transient Response

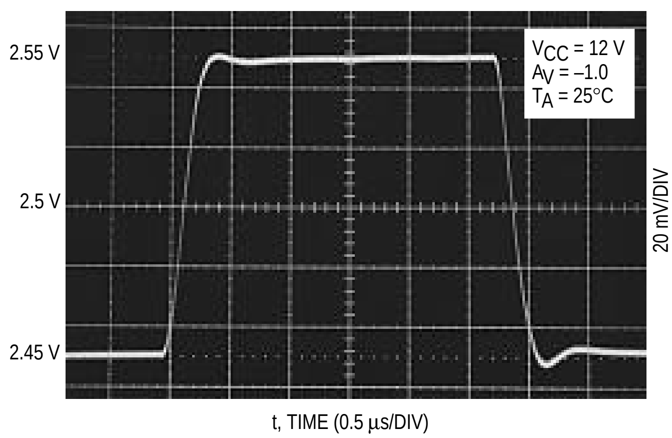


Figure 6. Error Amp Large Signal Transient Response

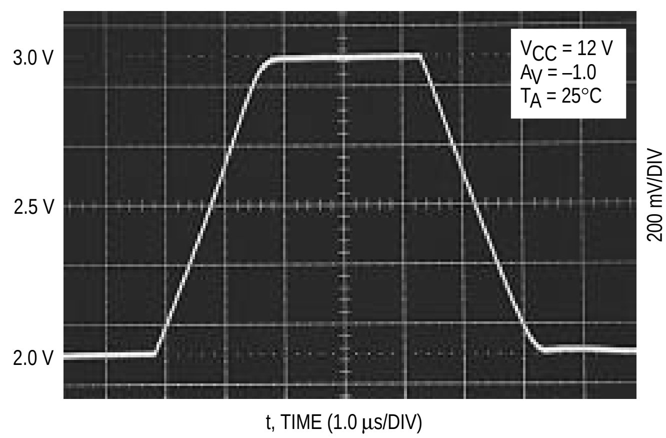


Figure 7. Error Amp Open Loop Gain and Phase versus Frequency

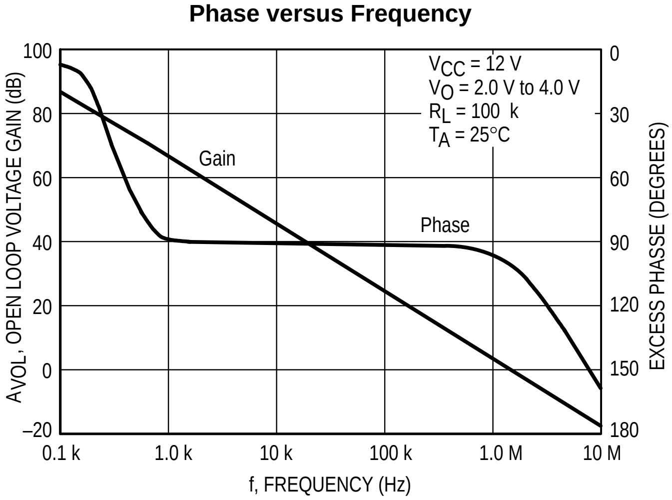


Figure 8. Current Sense Input Threshold versus Error Amp Output Voltage

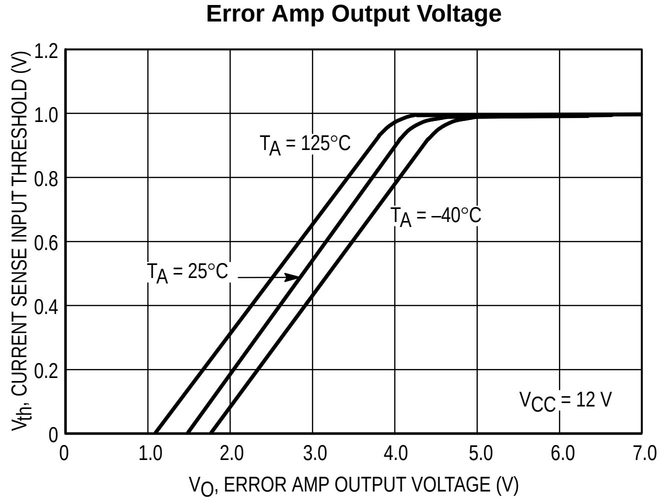


Figure 9. Voltage Feedback Input, Voltage versus Current

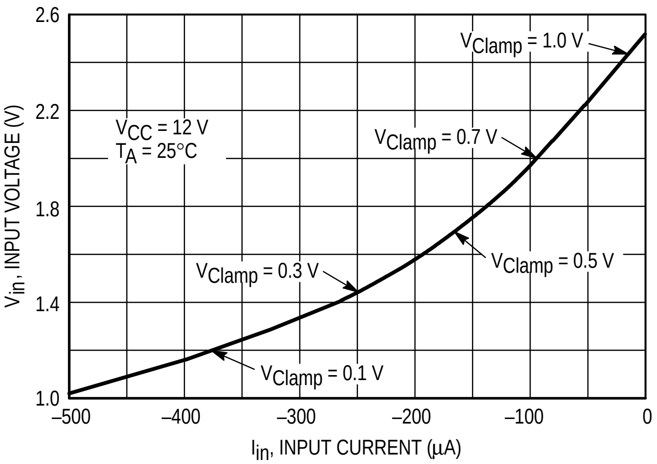


Figure 10. Voltage Feedback Input versus Current Sense Clamp Level

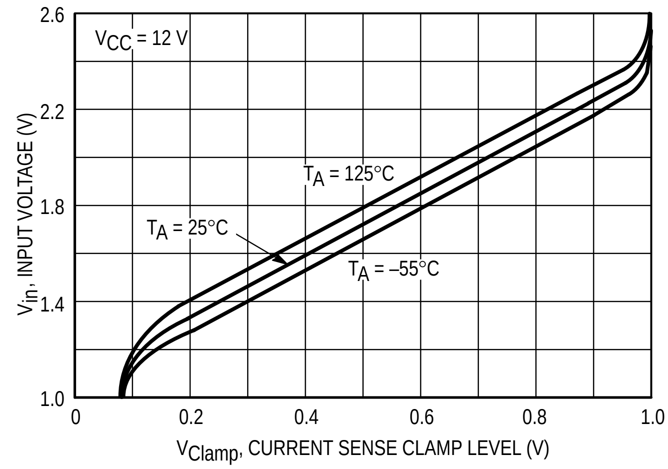


Figure 11. Reference Short Circuit Current versus Temperature

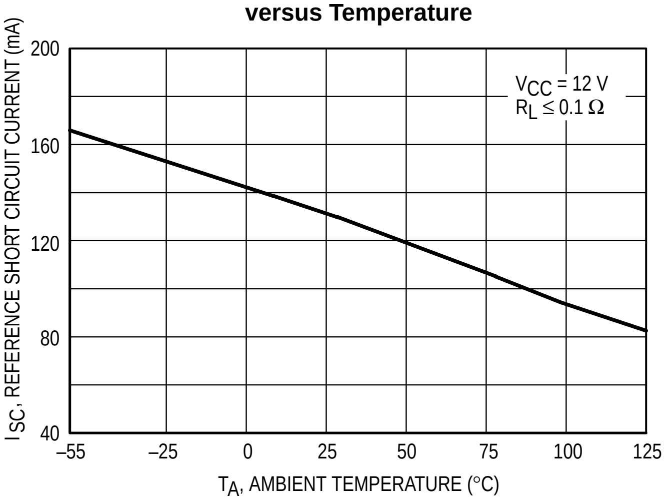


Figure 12. Reference Line and Load Regulation versus Temperature

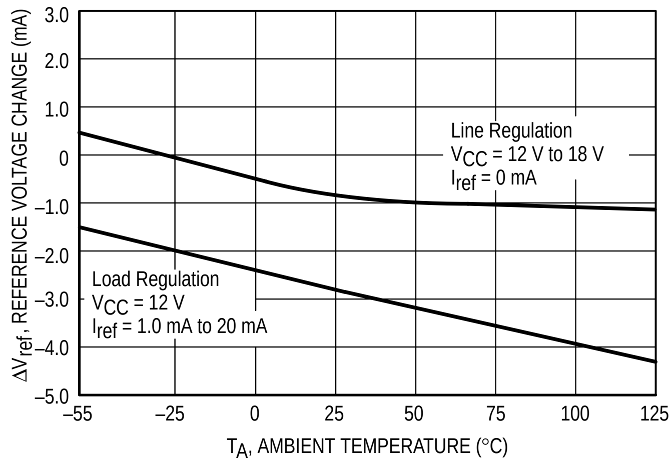


Figure 13. Reference Voltage Change versus Source Current

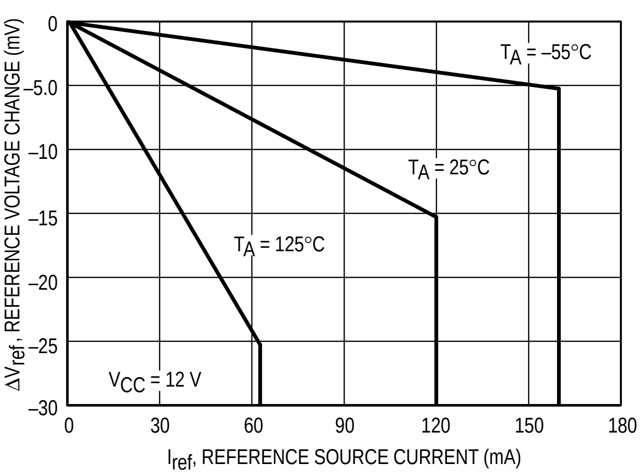


Figure 14. Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

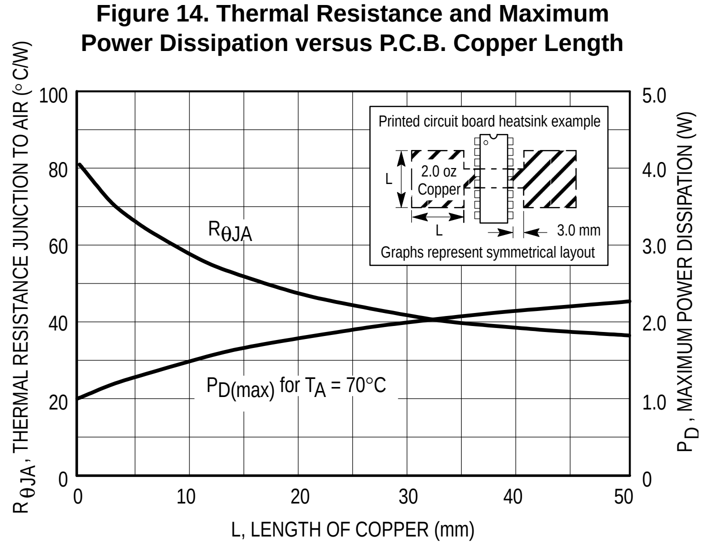


Figure 15. Output Waveform

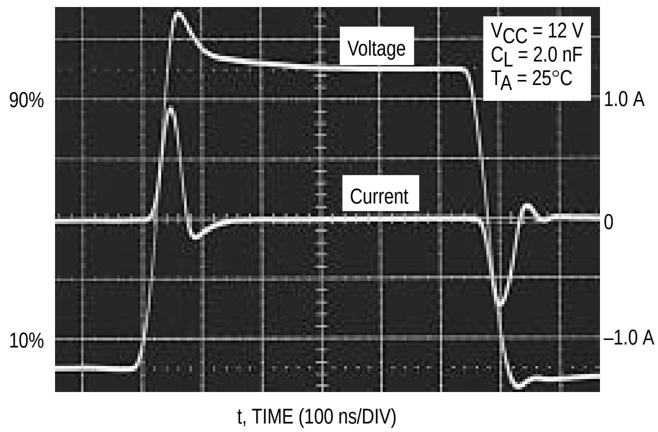


Figure 16. Output Cross Conduction

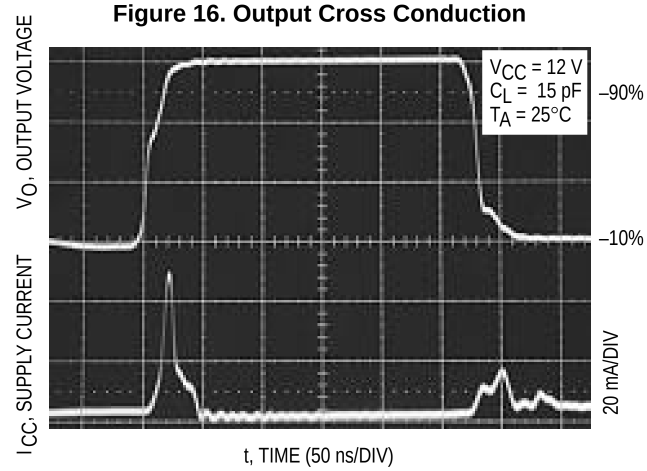


Figure 17. Sink Output Saturation Voltage versus Sink Current

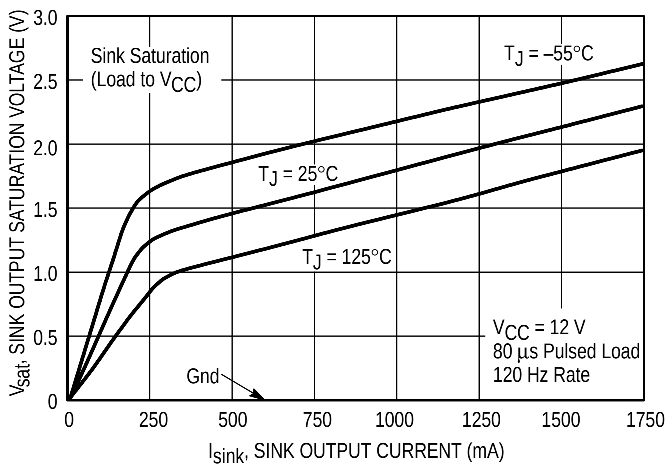


Figure 18. Source Output Saturation Voltage versus Load Current

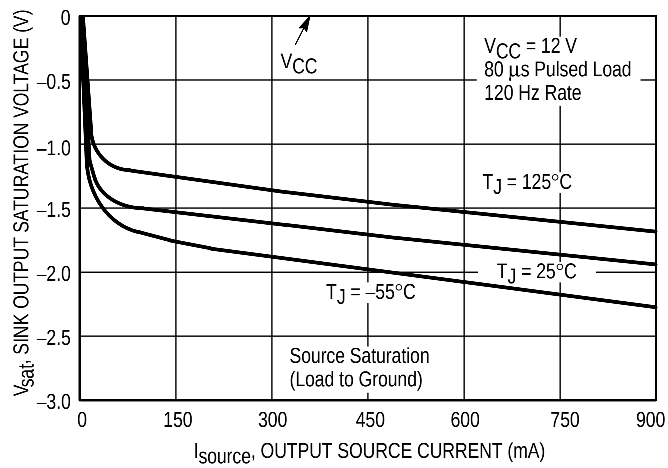


Figure 19. Supply Current versus Supply Voltage

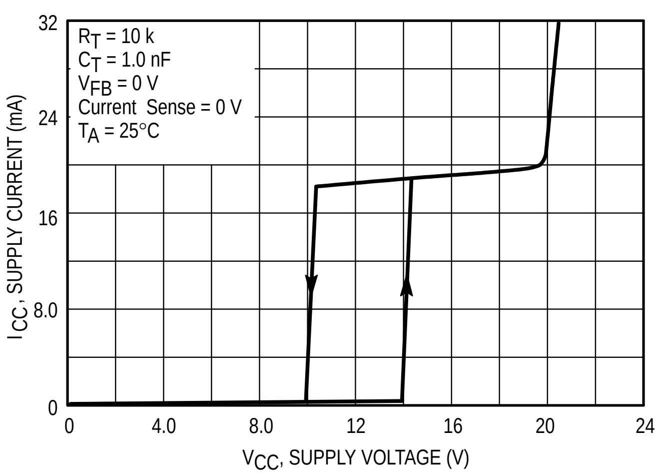


Figure 20. Power Supply Zener Voltage versus Temperature

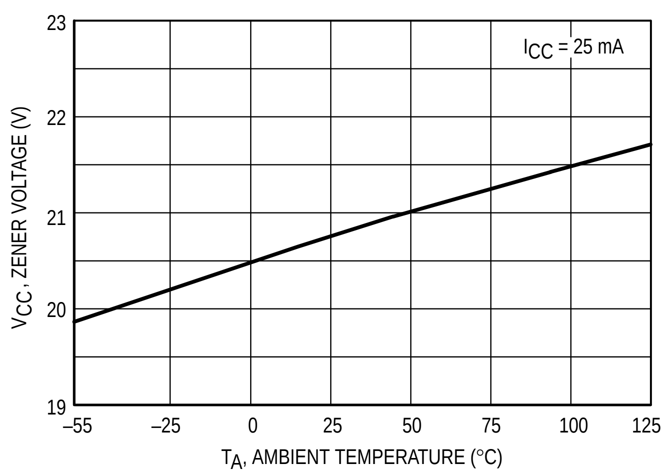


Figure 21. Valid Load Comparator Threshold versus Temperature

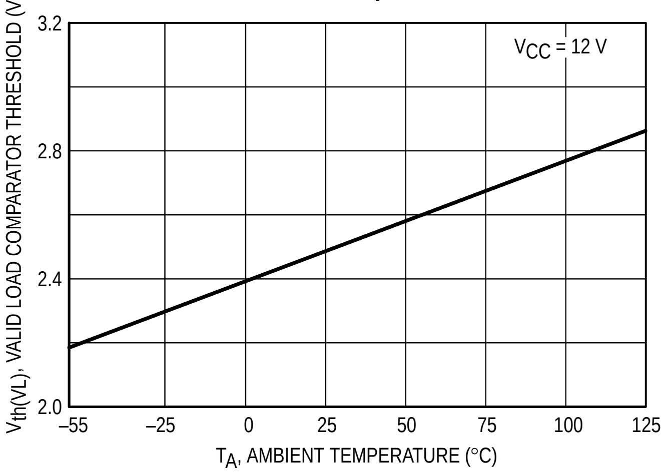


Figure 22. Demag Comparator Threshold versus Temperature

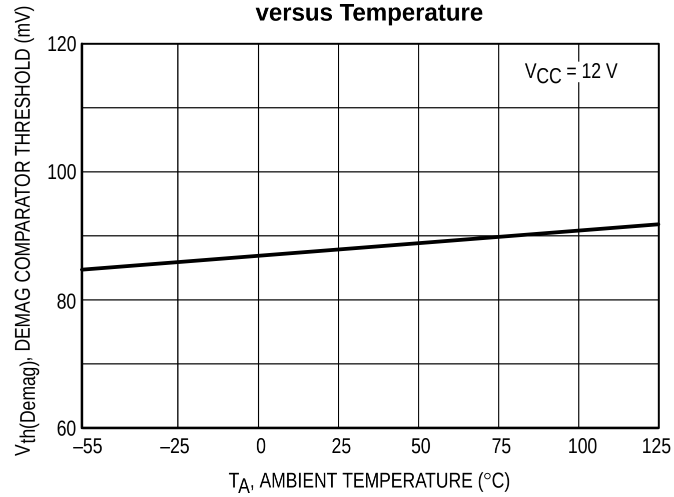


Figure 23. Load Detect Input Propagation Delay versus Temperature

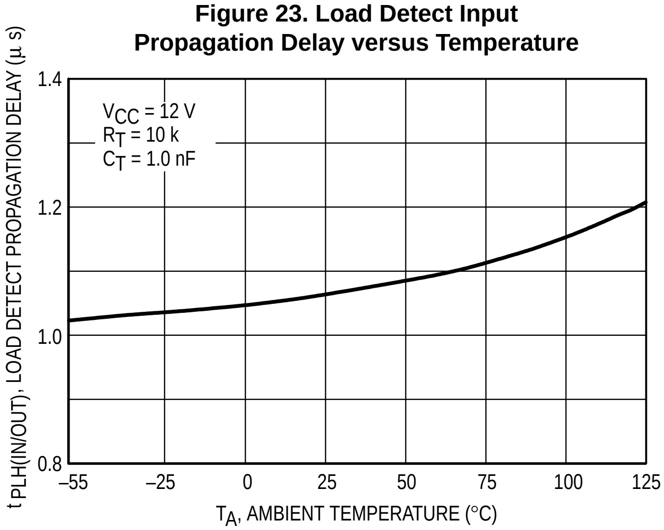


Figure 24. Startup Threshold Voltage versus Temperature

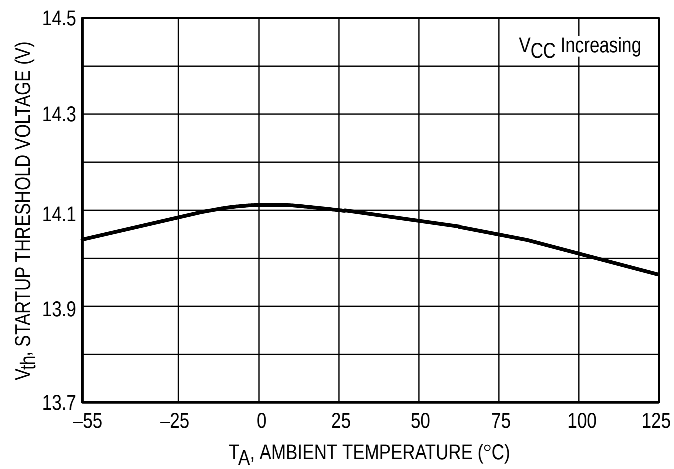


Figure 25. Minimum Operating Voltage After Turn–On versus Temperature

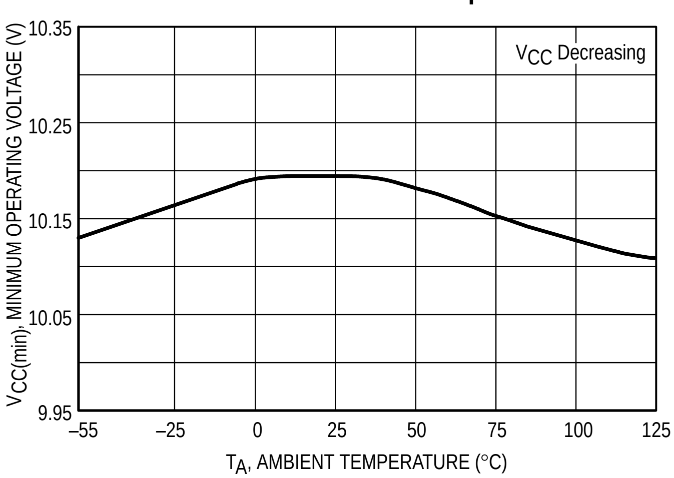


Figure 26. Reference Undervoltage Threshold versus Temperature

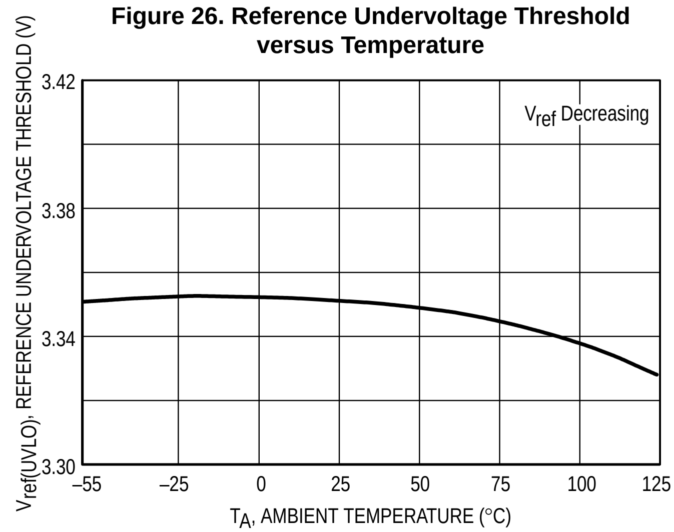


Figure 27. Representative Block Diagram

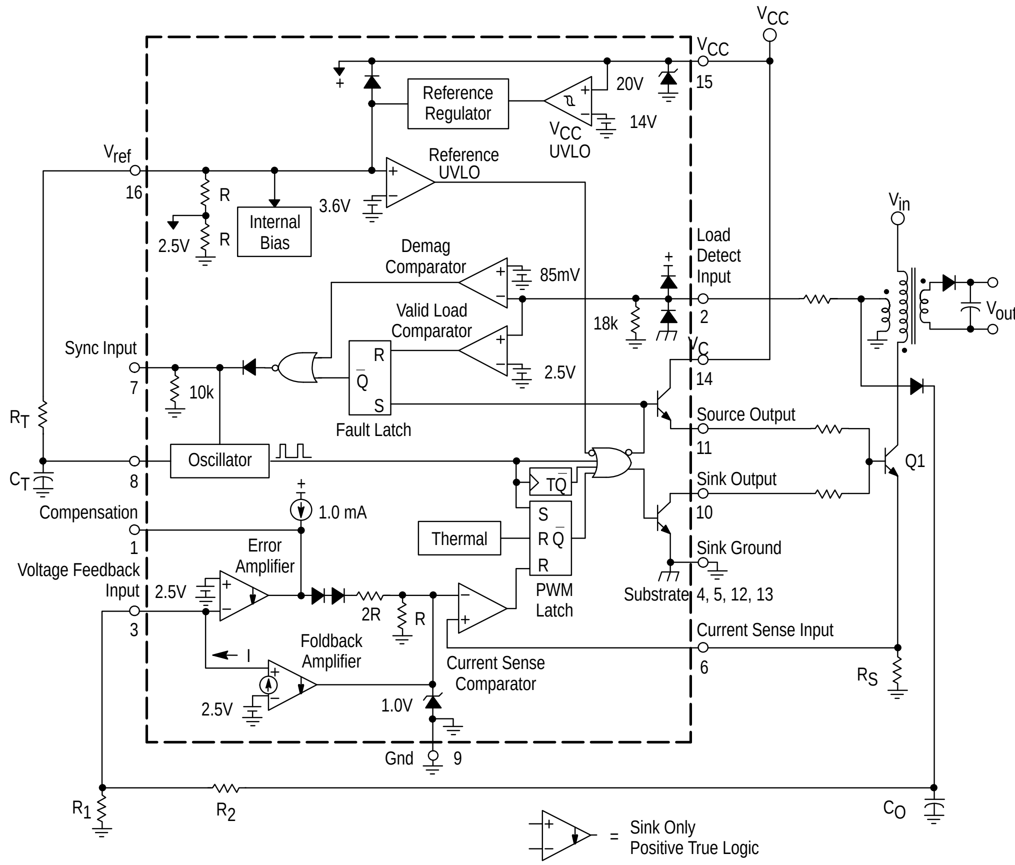
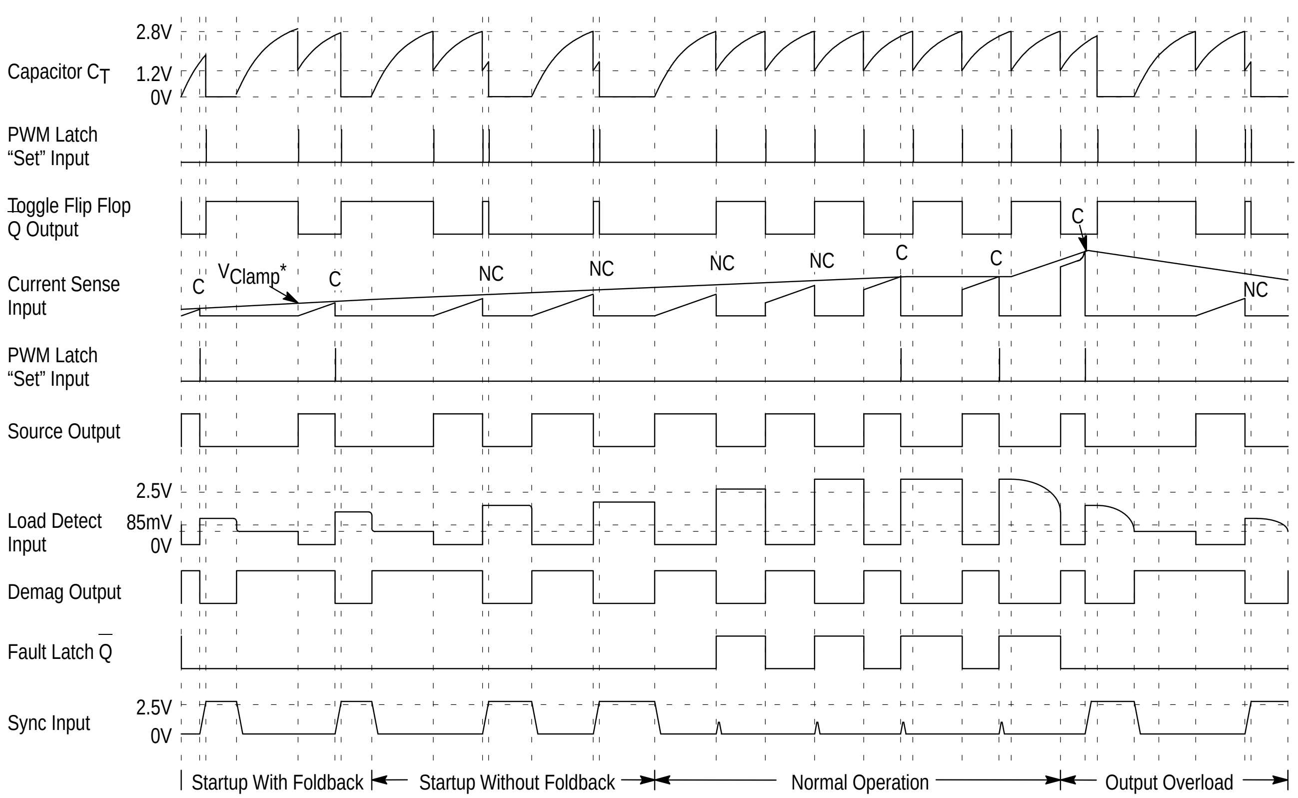


Figure 28. Timing Diagram



*C = Comparison of Current Sense Input With V_{Clamp} NC = No Comparison of Current Sense Input With V_{Clamp}

OPERATING DESCRIPTION

The MC44602 is a high performance, fixed frequency, current mode controller specifically designed to directly drive a bipolar power switch in off–line and high voltage dc–to–dc converter applications. This device offers the designer a cost effective solution with minimal external components. The representative block and timing diagrams are shown in Figures 27 and 28.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 5.0 V reference through resistor R_T to approximately 2.8 V and discharged to 1.2 V by an internal current sink. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds one of the inputs of the NOR gate high. This causes the Source and Sink outputs to be in a low state, thus producing a controlled amount of output deadtime. An internal toggle flip–flop has been incorporated in the MC44602 which blanks the output off every other clock cycle by holding one of the inputs of the NOR gate high. This in combination with the C_T discharge period yields output deadtimes programmable from 50% to 70%. Figure 1 shows R_T versus Oscillator Frequency and Figure 2, Output Deadtime versus Frequency, both for a given value of C_T. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency.

In many noise sensitive applications it may be desirable to frequency–lock the converter to an external system clock. This can be accomplished by applying a narrow rectangular clock signal with an amplitude of 3.2 V to 5.5 V to the Sync Input (Pin 7). For reliable locking, the free–running oscillator frequency should be set about 10% less than the clock frequency. If the clock signal is ac coupled through a capacitor, an external clamp diode may be required if the negative sync input current is greater than –5.0 mA. Connecting Pin 7 to V_{ref} will cause C_T to discharge to 0 V, inhibiting the Oscillator and conduction of the Source Output. Multi–unit synchronization can be accomplished by connecting the C_T pin of each IC to a single MC1455 timer.

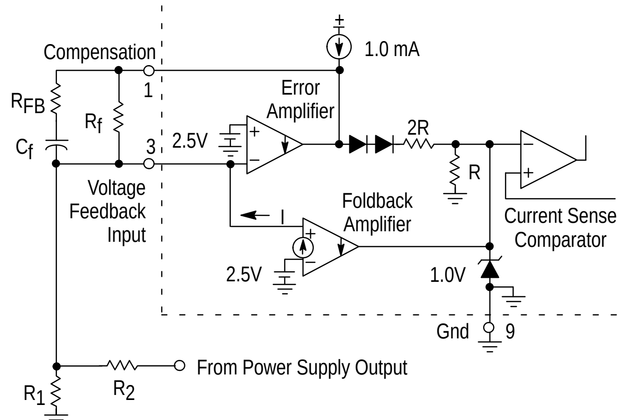
Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical dc voltage gain of 90 dB, and a unity gain bandwith of 1.0 MHz with 57 degrees of phase margin (Figure 7). The noninverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current with the inverting input at 2.5 V is –2.0 µA. This can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 1) is provided for external loop compensation (Figure 29). The output voltage is offset by two diodes drops (≈1.4 V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Source Output (Pin 11) when Pin 1 is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft–start interval. The Error Amp minimum feedback resistance is limited by the amplifier's minimum source current (0.5 mA) and the required output voltage (V_{OH}) to reach the comparator's 1.0 V clamp level:

$$R_{f(min)} \approx \frac{3.0\ (1.0\ V)\ +\ 1.4\ V}{0.5mA} = 8800\ \Omega$$

Figure 29. Error Amplifier Compensation



Current Sense Comparator and PWM Latch

The MC44602 operates as a current mode controller, where output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier output (Pin 1). Thus the error signal controls the peak inductor current on a cycle–by–cycle basis. The Current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Source Output during the appropriate oscillator cycle. The inductor current is converted to a voltage by inserting the ground referenced sense resistor R_S in series with the emitter of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 6) and compared to a level derived from the Error Amp output. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 1 where:

$$I_{pk} \approx \frac{V_{(Pin1)} - 1.4V}{3\ R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} \approx \frac{1.0\ V}{R_S}$$

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and the output rectifier recovery time. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability; refer to Figure 30.

Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built–in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 14.1 V/10.2 V. The V_{ref} comparator upper and lower thresholds are 3.6 V/3.3 V. The large hysteresis and low startup current of the MC44602 make it ideally suited for off–line converter applications (Figures 33, 34) where efficient bootstrap startup techniques are required.

A 20 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC from excessive voltage that can occur during system startup. The upper limit for the minimum operating voltage of the MC44602 is 11V.

Outputs

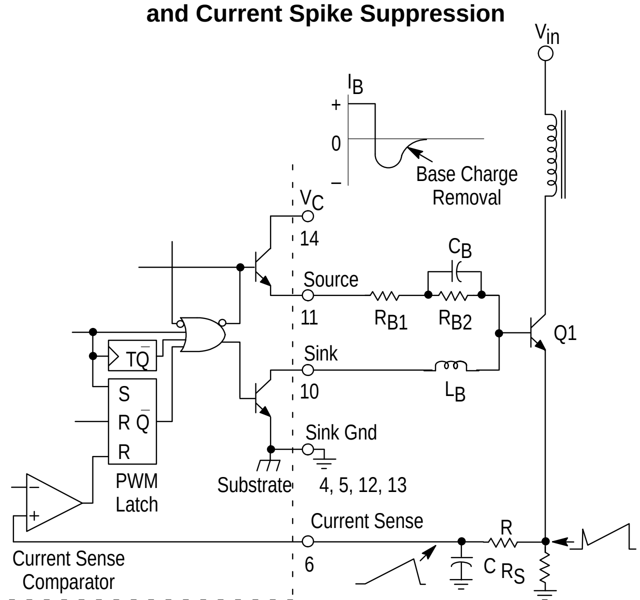
The MC44602 contains a high current split totem pole output that was specifically designed for direct drive of Bipolar Power Transistors. By splitting the totem pole into separate source and sink outputs, the power supply designer has the ability to independently adjust the turn–on and turn–off base drive to the external power transistor for optimal switching. The Source and Sink outputs are capable of up to 1.0 A and 1.5 A respectively and feature 50 ns switching times with a 1.0 nF load. Additional internal circuitry has been added to keep the Source Output “Off” and the Sink Output “On” whenever an undervoltage lockout is active. This feature eliminates the need for an external pull–down resistor and guarantees that the power transistor will be held in the “Off” state.

Separate output stage power and ground pins are provided to give the designer added flexibility in tailoring the base drive circuitry for a specific application. The Source Output high–state is controlled by applying a positive voltage to V_C (Pin 14) and is independent of V_{CC}. A zener clamp is typically connected to this input when driving power MOSFETs in systems where V_{CC} is greater than 20V. The Sink Output low–state is controlled by applying a negative voltage to the Sink Ground (Pins 4, 5, 12, 13). The Sink Ground can be biased as much as 5.0 V negative with respect to Ground (Pin 7). Proper implementation of the V_C and Sink Ground pins will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level.

Reference

The 5.0 V bandgap reference has a tolerance of ±6.0% over a junction temperature range of –25°C to 85°C. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short circuit protection and is capable of providing in excess of 20 mA for powering additional control system circuitry.

Figure 30. Bipolar Transistor Drive and Current Spike Suppression



Thermal Protection and Package

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 160°C, the PWM Latch is held in the “reset” state, forcing the Source Output “Off” and the Sink Output “On”. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a substitute for proper heatsinking.

The MC44602 is contained in a heatsinkable 16–lead plastic dual–in–line package in which the die is mounted on a special heat tab copper alloy lead frame. This tab consists of the four center Sink Ground pins that are specifically designed to improve the thermal conduction from the die to the circuit board. Figure 14 shows a simple and effective method of utilizing the printed circuit medium as a heat dissipater by soldering these pins to an adequate area of copper foil. This permits the use of standard layout and mounting practices while having the ability to halve the junction to air thermal resistance. This example is for a symmetrical layout on a single–sided board with two ounce per square foot of copper.

Design Considerations

Do not attempt to construct the converter on wire–wrap or plug–in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse–width jitter. This is usually caused by excessive noise pick–up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low–current signal, and high current switch and output grounds returning on separate

paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 µF) connected directly to V_{CC}, V_C, and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise generating components.

PROTECTION MODES

The MC44602 operates as a conventional fixed frequency current mode controller when the power supply output load is less than the design limit. For enhanced system reliability, this device has the unique ability of changing operating modes if the power supply output is overloaded or shorted.

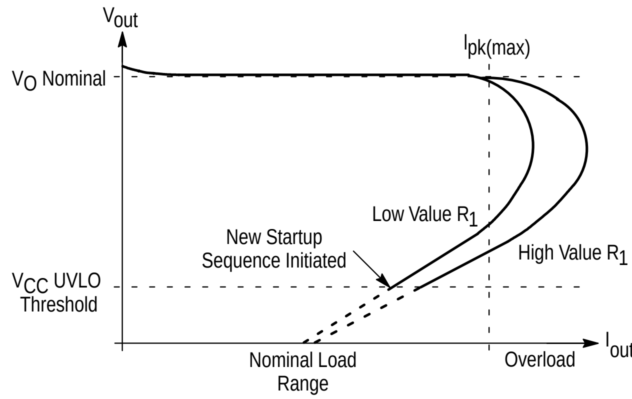
Overload Protection

Power supply overload protection is provided by the Foldback Amplifier. As the output load gradually increases, the Error Amplifier senses that the voltage at Pin 3 is less than the 2.5 V threshold. This causes the voltage at Pin 1 to rise, increasing the Current Sense Comparator threshold in order to maintain output regulation. As the load further increases, the inverting input of the Current Sense Comparator reaches the internal 1.0 V clamp level, limiting the switch current to the calculated $I_{pk(max)}$. At this point any further increase in load will cause the power supply output to fall out of regulation. As the voltage at Pin 3 falls below 2.5 V, current will flow out of the Foldback Amplifier input, and the internal clamp level will be proportionally reduced (Figures 9, 10). The increase in current flowing out of the Foldback Amplifier input in conjunction with the reduced clamp level, causes the power supply output voltage to fall at a faster rate than the voltage at Pin 3. This results in the output foldback characteristic shown in Figure 31. The shape of the current limit "knee" can be modified by the value of resistor R_1 in the feedback divider. Lower values of R_1 will reduce the $I_{pk(max)}$ clamp level at a faster rate.

Improper operation of the Foldback Amp can be encountered when the Error Amp compensation capacitor C_f exceeds 2.0 nF. The problem appears at Startup when the output voltage of the power supply is below nominal, causing the Error Amp output to rise quickly. The rapid change in output voltage will be coupled through C_f to the Inverting Input (Pin 3), keeping it at its 2.5 V threshold as the 1.0 mA Error Amp current source charges C_f. This has the effect of disabling the Foldback Amp by preventing Pin 3 and the clamp level at the inverting input of the Current Sense Comparator, from rising in proportion to the power supply output voltage. By adding resistor R_{FB} in series with C_f, the voltage at Pin 3 can be held to 1.0 V, corresponding to a Current Sense clamp level of 0.08 V (Figure 10), while allowing the Error Amp output to reach its high state V_{OH} of 7.0 V. The required resistor to keep Pin 3 below 1.0 V during initial Startup is:

$$\frac{R_{FB}\,R_f}{R_{FB} + R_f} \geq 6\left(\frac{R_1\,R_2}{R_1 + R_2}\right)$$

Figure 31. Output Foldback Characteristic



Short Circuit Protection

Short circuit protection for the power supply is provided by the Valid Load Comparator, Fault Latch, and Demag Comparator. Figure 32 shows the logic truth table of the functional blocks. When operating the power supply with nominal output loading, the Fault Latch is "Set" by the NOR gate driver during the Power Transistor "On" time and "Reset" by the Fault Comparator during the "Off" time. When a severe overload or short circuit occurs on any output, the voltage during the "Off" time (flyback voltage) at the Load Detect Input, is unable to reach the 2.5 V threshold of the Valid Load Comparator. This causes the Fault Latch to remain in the "Set" state with output Q "Low". During the "Off" time the Demag Comparator output will also be "Low". This causes the NOR gate to internally hold the Sync Input "High", inhibiting the next fixed frequency Oscillator cycle and switching of the Power Transistor. As the load dissipates the stored transformer energy, the voltage at the Load Detect Input will fall. When this voltage reaches 85 mV, the Demag Comparator output goes "High", allowing the Sync Input to go "Low", and the Power Transistor to turn "On".

Note that as long as there is an output short, the switching frequency will shift to a much lower frequency than that set by R_T/C_T. The frequency shift has the effect of lowering the duty cycle, resulting in a significant reduction in Power Transistor and Output Rectifier heating when compared to conventional current mode controllers. The extended "On" time is the result of C_T charging from 0 V to 2.8 V instead of 1.2 V to 2.8 V. The extended "Off" time is the result of the output short time constant. The time constant consists of the output filter capacitance, and the equivalent series resistance (ESR) of the capacitor plus the associated wire resistance.

Figure 32. Logic Truth Table of Functional Blocks

Output Load	Power Transistor	Demag		Fault Latch			Sync	Operating Comments
		Input	Out	S	R	$\overline{Q}$	Input	
Nominal	On	<85mV	1	1	0	0	0	NOR gate driver sets Fault Latch.
	At Turn–Off	>85 mV, <2.5 V	0	0	0	0		Narrow spike at Sync Input (<2.5 V) as transformer voltage rises quickly, Oscillator is not affected.
	Off	>2.5 V	0	0	1	1	0	Valid Load Comparator resets Fault Latch.
Short	On	<85 mV	1	1	0	0	0	Short is not detected until transistor turn–off.
	At Turn–Off	>85 mV, <2.5 V	0	0	0	0	1	Valid Load Comparator fails to reset Fault Latch, Pulse at Sync Input exceeds 2.5 V, Oscillator is disabled.
	Off	<85 mV	1	0	0	0	0	Load dissipates transformer energy, Oscillator enabled.

During the initial power supply startup the controller sequences through the Short Circuit and Overload Protection modes as the output filter capacitors charge–up. If an output is shorted and the auxiliary feedback winding is used to power the control IC as in Figure 33, the V_{CC} UVLO lower threshold level will be reached after several cycles, disabling the IC and initiating a new startup sequence. The Short Circuit Protection mode can be disabled by grounding the Sync Input. Narrow switching spikes are present on this pin during normal operation. These spikes are caused by the rise time of the flyback voltage from the 85 mV Demag Comparator threshold to the 2.5 V Valid Load Comparator threshold. In high power applications, the increased negative current at the Load Detect Input can extend the switching spikes to the point where they exceed the Sync Input threshold. This problem can be eliminated by placing an external small signal clamp diode at the Load Detect Input. The diode is connected with the cathode at Pin 2 and the anode at ground.

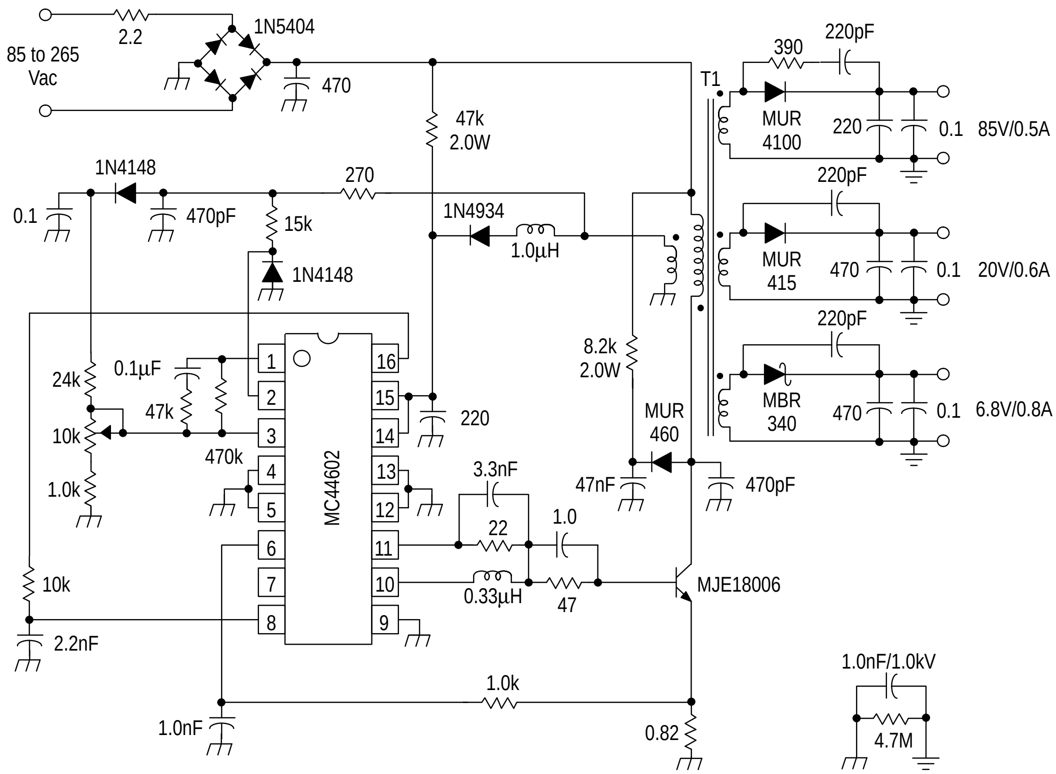
The divide–by–two toggle flip–flop will appear not to function properly during power supply startup without foldback, or operation with an overloaded output. This phenomena appears at the end of the oscillator cycle if there was not a current sense comparison, and after the flyback voltage at the Load Detect Input failed to exceed 2.5 V. Under these conditions, the Sync input will go high approximately 1.0 µs after the Load Detect Input exceeds the 85 mV Demag Comparator threshold. This causes C_T to discharge down towards ground, generating a second negative going edge on the oscillator waveform. This second edge results in the divide–by–two flip–flop being clocked twice for each “On” time of the switch transistor. During initial startup, this effect can be eliminated by insuring that the Foldback Amplifier is fully active with the addition of resistor R_{FB}. With the Foldback Amplifier active, the clamp level at the inverting input of the Current Sense Comparator will be low, allowing a comparison to take place during the switch transistor “On” time. When the Load Detect Input exceeds 85 mV, the Sync Input will go high, discharging C_T to ground after 1.0 µs, thus eliminating the second negative edge. Operation with the output overloaded will cause the toggle flip–flop to be clocked twice for each “On” time. This should not be a problem since the next “On” time is delayed by the Demag Comparator until the load dissipates the transformers energy.

The point where the IC detects that there is a severe output overload, or that the transformer has reached zero current, is controlled by the voltage of the auxiliary winding and a resistor divider. The divider consists of an external series resistor and an internal shunt resistor. The shunt resistor is nominally 18 kΩ but can range from 12 kΩ to 30 kΩ due to process variations. If more precise overload and zero current detection is required, the internal resistor variations can be swamped out by connecting a low value external resistor (≤2.7 kΩ) from Pin 2 to ground.

PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	Compensation	This pin is the Error Amplifier output and is made available for loop compensation.
2	Load Detect Input	A voltage indicating a severe overload or short circuit condition at any output of the switching power supply is connected to this input. The Oscillator is controlled by this information making the power supply short circuit proof.
3	Voltage Feedback Input	This is the inverting input of the Error Amplifier and the noninverting input of the Foldback Amplifier. It is normally connected to the switching power supply output through a resistor divider.
4, 5, 12, 13	Sink Ground	The Sink Ground pins form a single power return that is typically connected back to the power source on a separate path from Pin 9 Ground, to reduce the effects of switching transient noise on the control circuitry. These pins can be used to enhance the package power capabilities (Figure 14). The Sink Output low state (V_{OL}) can be modified by applying a negative voltage to these pins with respect to Ground (Pin 9) to optimize turn–off of a bipolar junction transistor.
6	Current Sense Input	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate conduction of the output switch transistor.
7	Sync Input	A narrow rectangular waveform applied to this input will synchronize the Oscillator. A dc voltage within the range of 3.2 V to 5.5 V will inhibit the Oscillator.
8	R_T/C_T	The Oscillator frequency and maximum Output duty cycle are programmed at this pin by connecting resistor R_T to V_{ref} and capacitor C_T to ground.
9	Ground	This pin is the control circuitry ground and is typically connected back to the power source on a separate path from the Sink Ground (Pins 4, 5, 12, 13).
10	Sink Output	Peak currents up to 1.5 A are sunk by this output suiting it ideally for turning–off a bipolar junction transistor. The output switches at one–half the oscillator frequency.
11	Source Output	Peak currents up to 1.0 A are sourced by this output suiting it ideally for turning–on a bipolar junction transistor. The output switches at one–half the oscillator frequency.
14	V_C	The Output high state (V_{OH}) is set by the voltage applied to this pin. With a separate connection to the power source, it can reduce the effects of switching transient noise on the control circuitry.
15	V_{CC}	This pin is the positive supply of the control IC. The minimum operating voltage range after startup is 11 V to 18 V.
16	V_{ref}	This is the 5.0 V reference output. It provides charging current for capacitor C_T through resistor R_T and can be used to bias any additional system circuitry.

Figure 33. 60 Watt Off–Line Flyback Regulator



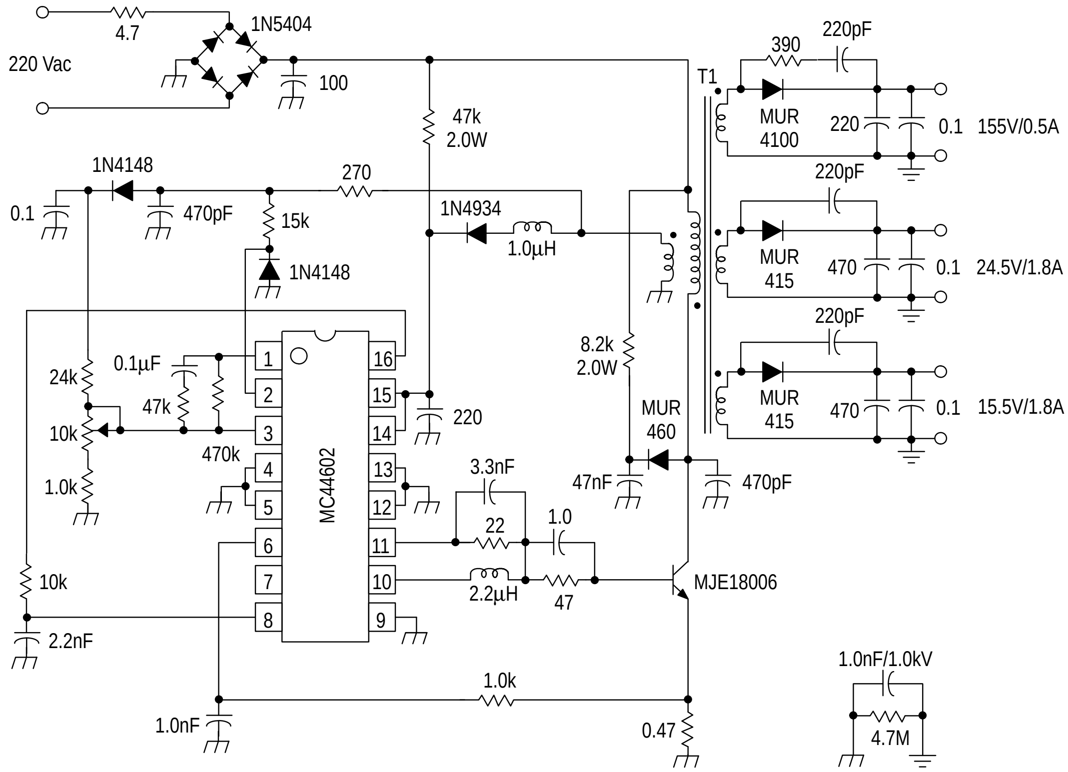
Test	Conditions	Results
Line Regulation	V_{in} = 85 Vac to 265 Vac	
85V	I_O = 0.5 A	Δ = 1.0 V or ± 0.6%
20V	I_O = 0.5 A	Δ = 0.04 V or ± 0.1%
6.8V	I_O = 0.8 A	Δ = 0.07 V or ± 0.5%
Load Regulation	V_{in} = 220 Vac	
85V	I_O = 0.1 A to 0.5 A	Δ = 1.0 V or ± 0.6%
20V	I_O = 0.1 A to 0.5 A	Δ = 0.4 V or ± 1.0%
6.8V	I_O = 0.1 A to 0.8 A	Δ = 0.2 V or ± 1.5%
Efficiency	V_{in} = 110 Vac, P_O = 58 W	81%
Standby Power	V_{in} = 110 Vac, P_O = 0 W	2.0 W

T1 – Orega SMT2 (G4787–01)
Primary: 41 Turns, #25AWG
Auxiliary Feedback: 12 Turns, #25AWG
Secondary: 85 V – 60 Turns, #25AWG
20 V – 15 Turns, #25AWG (2 Strands) Bifiliar Wound
6.8 V – 5 Turns, #25AWG (2 Strands) Bifiliar Wound

Core – ETD39 34x17x11 B52

Gap – ≈ 0.020″ for a primary inductance of 750 µH, A_L = 500 nH/Turn^2

Figure 34. 150 Watt Off–Line Flyback Regulator



Test	Conditions	Results
Line Regulation	V_{in} = 185 Vac to 265 Vac	
155V	I_O = 0.5 A	Δ = 1.0 V or ± 0.3%
24.5V	I_O = 1.0. A	Δ = 0.4 V or ± 0.8%
15.5V	I_O = 1.0 A	Δ = 0.3 V or ± 1.0%
Load Regulation	V_{in} = 220 Vac	
155V	I_O = 0.1 A to 0.5 A	Δ = 2.0 V or ± 0.7%
24.5V	I_O = 0.1 A to 1.0 A	Δ = 0.4 V or ± 0.8%
15.5V	I_O = 0.1 A to 1.0 A	Δ = 0.2 V or ± 0.7%
Efficiency	V_{in} = 220 Vac, P_O = 117.5 W	83%
Standby Power	V_{in} = 220 Vac, P_O = 0 W	5.0 W

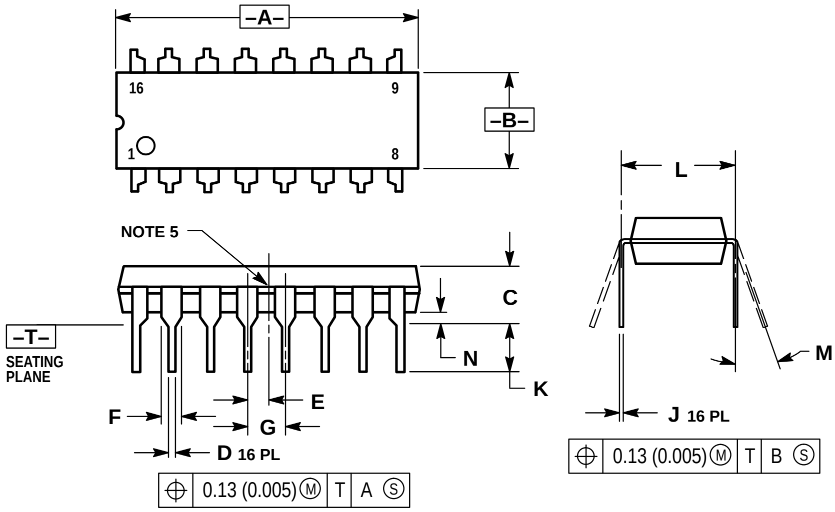
T1 – Orega SMT2 (G4717–01)
Primary: 55 Turns, #25AWG
Auxiliary Feedback: 6 Turns, #25AWG
Secondary: 155 V – 52 Turns, #25AWG
24.5 V – 9 Turns, #25AWG (2 Strands) Bifiliar Wound
15.5 V – 6 Turns, #25AWG (2 Strands) Bifiliar Wound

Core – GETV 53x18x18 B52

Gap – ≈ 0.020″ for a primary inductance of 1.35 µH, A_L = 450 nH/Turn^2

OUTLINE DIMENSIONS

P2 SUFFIX
PLASTIC PACKAGE
CASE 648C–03
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. INTERNAL LEAD CONNECTION BETWEEN 4 AND 5, 12 AND 13.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.840	18.80	21.34
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
E	0.050 BSC		1.27 BSC	
F	0.040	0.70	1.02	1.78
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.040	0.39	1.01

How to reach us:
USA / EUROPE: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE (602) 244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, Toshikatsu Otsuki,
6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298